WHAT IS CLAIMED IS:

1. A method for transferring data in parallel from an external memory device to an integrated circuit, the method comprising:

transferring a start read address from the integrated circuit to the external memory device;

providing a clock signal generated by the integrated circuit to the external memory device;

sequentially generating read addresses in response to the clock signal beginning with the start read address using an address counter in the external memory device;

reading data stored in the external memory device at the read addresses; and

transferring the data in parallel from the external memory device to the integrated circuit.

2. The method as defined in claim 1 further comprising:

resetting a read address to the start read address when an output enable signal generated by the integrated circuit has a first voltage,

wherein the address counter increments the read address in response to the clock signal when the output enable signal has a second voltage.

3. The method as defined in claim 1 wherein the external memory device operates in sequential read mode when the clock signal toggles.

4. The method as defined in claim 1 wherein the external memory device operates in sequential read mode when the integrated circuit sends a sequential read command to the external memory device.

5. The method as defined in claim 1 wherein the integrated circuit is a first programmable integrated circuit that is coupled in series with a plurality of cascaded programmable integrated circuits, and data is transferred in parallel from the external memory device to the cascaded programmable integrated circuits.

6. The method as defined in claim 5 wherein the first programmable integrated circuit is a master device that controls the transfer of the data from the external memory device to the cascaded programmable integrated circuits.

7. The method as defined in claim 1 wherein the integrated circuit is a field programmable gate array and the data is configuration data.

8. The method as defined in claim 1 wherein the integrated circuit is a programmable integrated circuit that is part of a digital system that includes a microprocessor.

9. The method as defined in claim 1 wherein the data is transferred in parallel from the external memory device to the integrated circuit along 8 parallel signal lines.

10. The method as defined in claim 1 wherein the data is transferred in parallel from the external memory device to the integrated circuit along 16 parallel signal lines.

11. The method as defined in claim 1 wherein the external memory device is a FLASH memory.

12. A system for transferring data to an integrated circuit, the system comprising:

an integrated circuit that generates a start read address and a clock signal; and

an external memory device including an address counter that sequentially generates read addresses beginning with the start read address in response to the clock signal, that accesses data stored in a memory array at the read addresses, and that transfers the accessed data along parallel signal lines to the integrated circuit.

13. The system according to claim 12 wherein the address counter resets a read address to the start read address when an output enable signal generated by the integrated circuit has a first voltage, and the address counter increments the read address in response to the clock signal when the output enable signal has a second voltage.

14. The system according to claim 12 wherein the external memory device operates in sequential read mode when the clock signal toggles.

15. The method as defined in claim 12 wherein the external memory device operates in sequential read mode when the integrated circuit sends a sequential read command to the external memory device.

16. The system according to claim 12 wherein the integrated circuit is a first programmable integrated circuit that is coupled in series with a plurality cascaded programmable integrated circuits, and data is transferred in parallel from the external memory device to the cascaded programmable integrated circuits.

17. The system according to claim 16 wherein the first programmable integrated circuit is a master device that controls the transfer of the data from the external memory device to the cascaded programmable integrated circuits.

18. The system according to claim 12 wherein the integrated circuit is a field programmable gate array and the data is configuration data.

19. The system according to claim 12 wherein the integrated circuit is a programmable integrated circuit that is part of a digital system including a microprocessor.

20. The system according to claim 12 wherein the accessed data is transferred in parallel from the external memory device to the integrated circuit along 8 parallel signal lines.

21. The system according to claim 12 wherein the accessed data is transferred in parallel from the external memory device to the integrated circuit along 16 parallel signal lines.

22. The system according to claim 12 wherein the external memory device is a FLASH memory.